What is claimed is:

1. In a semiconductor device wherein conductive interconnection members are inlaid into and separated at a surface by a dilectric member, the spacing of said conductive interconnection members at said surface being in the sub 250 nanometer range, and said conductive interconnection members exhibiting high electric field concentrations at said surface,

an improvement comprising:

a mask member extending over all of said dielectric member from a first conductive interconnection member to a second conductive interconnection member,

said mask member being positioned in contact with said dielectric member and intersecting said conductive interconnection members at a location that is separated from said surface.

2. The improvement of claim 1 wherein the material of said conductive interconnection members is at least one member of the group comprising copper, aluminum, silver, gold and alloys thereof.

3. The improvement of claim 2 wherein the material of said mask member is a at least one material taken from the group of amorphous silicon, carbon, hydrogen (α - Si:C:H); silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen, carbon alloys (Si:N:C); silicon nitride(Si_3N_4); silicon dioxide(SiO_2); and , silicon oxynitride (SiON).

4. The improvement of claim 1 wherein said mask member has a thickness related to the capacitance of said conductive interconnect members.

5. The improvement of claim 1 wherein said location of said mask member intersecting with said conductive interconnect members is separated from said surface a distance in the range of 1 to 20 nanometers.

6. The improvement of claim 5 wherein said location of said mask member intersecting said conductive interconnect members is separated from said surface a distance of 5 nanometers.

7. The improvement of claim 6 wherein said conductive interconnect members in said dielectric member are surrounded by an electrically conductive diffusion barrier liner.

8. The improvement of claim 7 wherein said liner is of a material taken from the group of at least one of Ta, Ti, TaN, TiN, W and WN.

9. A semiconductor device wherein conductive interconnection members are inlaid into and separated at a surface of a bulk dielectric member, the spacing of said conductive interconnection members at said surface being in the sub 250 nanometer range, and said conductive interconnection members exhibiting high electric field concentrations at said surface,

an improvement comprising:

a mask member of at least one material taken from the group of amorphous silicon, carbon, hydrogen (α - Si:C:H); silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen, carbon alloys (Si:N:C); silicon nitride(Si_3N_4); silicon dioxide(SiO_2); and , silicon oxynitride (SiON); extending over all of said dielectric member from a first conductive interconnection member to a second conductive interconnection member,

said conductive interconnect members being of at least one material taken from the group of copper, aluminum, silver, gold and alloys thereof.

said mask member being positioned in contact with said dielectric member and intersecting said conductive interconnection members at a location that is separated from said surface.

10. The device of claim 9 wherein conductive interconnect members in said bulk polymer member are surrounded by an electrically conductive diffusion barrier liner.

11. The device of claim 9 wherein said liner is of a material taken from the group of at least one of Ta, Ti, TaN, TiN, W and WN.

12. A semiconductor device wherein conductive interconnection members are inlaid into and separated at a surface of a bulk dielectric member, the spacing of said conductive interconnection members at said surface being in the sub 250 nanometer range, and said conductive interconnection members exhibiting high electric field concentrations at said surface,

an improvement comprising:

said conductive interconnect members being of at least one material taken from the group of copper, aluminum, silver, gold and alloys thereof,

said conductive interconnect members extending above the surface of said intralevel dielectric a distance in the range of from 1 - 20 nanometers.

13. The device of claim 12 wherein said distance said conductive interconnect members extend above said surface of said intralevel dielectric is from 2 - 5 nanometers.

14 The process of preventing high electric field concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nanometer range size and spacing conductive interconnect members in said body, comprising the step of:

positioning a mask member of a material that is hardened relative to the hardness of said dielectric body surrounding at least one said conductive member and over at least a portion of said dielectric member at a location below said surface a distance defined by the beginning of said facetted portion.

15. The process of claim 14 wherein the material of said mask member is a material taken from the group of amorphous silicon, carbon, hydrogen (a-Si:C:H); silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen, carbon alloys (Si:N:C); silicon nitride(Si_3N_4); silicon dioxide(SiO_2); and , silicon oxynitride (SiON).

16. In a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface,
an improvement comprising the intermediate steps of:
depositing a diffusion barrier liner in the formation of said conductive interconnect members where said conductive interconnect members pass through said bulk dielectric, and then, employing said diffusion barrier liner as the conductor for plating in subsequent deposition of metal filling said conductive interconnect members.

17. The process improvement of claim 16 wherein the material of said diffusion barrier liner is a material taken from the group of at least one of Ta, Ti, TaN, TiN, W and WN, and said subsequently deposited metal is copper..

18. The process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric body and through a mask layer atop said dielectric to a common surface,
the improvement comprising the intermediate steps of:
etching trench and via shape openings out of said dielectric body through said mask layer in a region below said surface,
lining said openings with thin electrically conductive diffusion barrier layer,

coating said liner layer with a thin metal layer,

electroplating a thick metal into and filling said openings including overcoating said surface,

planarizing said overcoated surface through chemical - mechanical operations,and,

removing said mask layer in all portions between said openings to a depth that establishes a selected dimension of the upper surface of said mask below said surface.

19. The process of claim 18 wherein said mask layer is of at least one material taken from the group of amorphous silicon, carbon, hydrogen (-c- Si:C:H); silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen, carbon alloys (Si:N:C); silicon nitride(Si_3N_4); silicon dioxide($Si O_2$); and , silicon oxynitride (SiON).

20. The process of claim 19 wherein said thin electrically conducting diffusion barrier layer is of at least one material taken from the group of Ta, Ti, TaN, TiN, W and WN,

21. The process of claim 20 wherein said thick metal being electroplated into and filling said openings is of at least one metal taken from the group of copper, aluminum, silver, gold and alloys thereof.